DIGITAL PLL WITH GEAR SHIFT

ABSTRACT OF THE DISCLOSURE

A PLL synthesizer (100) includes a gear-shifting scheme of the PLL loop gain constant, α. During frequency/phase acquisition, a larger loop gain constant, α_1 is used such that the resulting phase error is within limits. After the frequency/phase gets acquired, the developed phase error, which is a rough indication of the frequency offset is in a steady-state condition. While transitioning into the tracking mode, the DC offset is added to the DCO tuning signal preferably the DC offset is added to the phase error signal and the loop constant is reduced from α_1 to α_2. This scheme provides for hitless operation, while requiring a low dynamic range of the phase detector (101).